# Instruction Manual

Tektronix

# TMS 532
# PPC405GP Microprocessor Support

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# General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

## Symbols and Terms

**Terms in this Manual.** These terms may appear in this manual:

***CAUTION.*** *Caution statements identify conditions or practices that could result in damage to this product or other property.*

**Terms on the Product.** These terms may appear on the product:

CAUTION indicates a hazard to property including the product.

**Symbols on the Product.** The following symbols may appear on the product:

CAUTION
Refer to Manual

# Preface

This instruction manual contains specific information about the TMS 532 PPC405GP microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 532 PPC405GP support was purchased, you only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you need to supplement this instruction manual with information on basic operations to set up and run the support. See Manual Conventions below for more information.

## Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help or a user manual covering the basic operations of a microprocessor support.

# Contacting Tektronix

| | |
|---|---|
| **Phone** | 1-800-833-9200* |
| **Address** | Tektronix, Inc.<br>Department or name (if known)<br>14200 SW Karl Braun Drive<br>P.O. Box 500<br>Beaverton, OR 97077<br>USA |
| **Web site** | www.tektronix.com |
| **Sales support** | 1-800-833-9200, select option 1* |
| **Service support** | 1-800-833-9200, select option 2* |
| **Technical support** | Email: techsupport@tektronix.com<br>1-800-833-9200, select option 3*<br>1-503-627-2400<br>6:00 a.m. – 5:00 p.m. Pacific time |

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
**Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.**

# Getting Started

# Getting Started

This section contains information on the TMS 532 PPC405GP microprocessor support package and information on connecting your logic analyzer to your system under test.

## Support Package Description

The TMS 532 PPC405GP microprocessor support package displays disassembled data from systems based on the IBM PPC405GP microprocessor.

The TMS 532 PPC405GP support includes the 405GPSDRAM software for the SDRAM Interface and the 405GPASYNC software for the 405GPASYNC Peripheral interface.

To use this support efficiently, you need to have the items listed in information on basic operations in your logic analyzer online help and *PPC405GP Controller Users Manual*: IBM, April 2000.

Information on basic operations in your online help also contains a general description of the support.

## Logic Analyzer Software Compatibility

The floppy disk label on the microprocessor support states which version of logic analyzer software this support is compatible with.

## Logic Analyzer Configuration

The TMS 532 PPC405GP support allows a choice of required minimum module configurations:

- 405GPASYNC support requires a minimum of one 102 channel module
- 405GPSDRAM support requires a minimum of one 68 channel module

To use both supports at the same time requires the above two modules. If you want to use only one support at a time, you must select the correct module and specify the support.

## Requirements and Restrictions

Review the general requirements and restrictions of microprocessor support packages in the information on basic operations as they pertain to your system under test.

Review electrical specifications in *Specifications* on page 3–1 as they pertain to your system under test, as well as the following descriptions of other TMS 532 PPC405GP support requirements and restrictions.

**System Clock Rate** The operating speeds that the TMS 532 PPC405GP support can acquire data from the PPC405GP microprocessor are listed on Table 3–1 on page 3–1. These specifications were valid at the time this manual was printed. Please contact your Tektronix Sales Representative for current information on the fastest devices supported.

**NonIntrusive Acquisition** Acquiring microprocessor bus cycles is nonintrusive to the system under test. That is, the PPC405GP support will not intercept, modify, or present signals back to the system under test.

## Functionality Not Tested

- DMA cycles (both supports)
- External Master cycles (both supports)
- Device paced cycles for 405GPASYNC
- Bus widths 16 and 32 for 405GPASYNC
- CAS latency 3 and 4 for 405GPSDRAM

## Functionality Not Supported

**Cache** The cache needs to be disabled for the disassembly to function correctly.

**Data** The data must be uncompressed or the supports will not disassembly correctly.

## Standard Accessories

The TMS 532 PPC405GP Support is shipped with the following standard accessories:

- TMS 532 PPC405GP Support SW Disk includes:

  405GPSDRAM interface
  405GPASYNC Peripheral interface

- *TMS 532 PPC405GP Support Instruction Manual*

## Options

The following options are available when ordering the TMS 532 PPC405GP Support:

- Option 21–Add P6434 Mass-Termination Probes (3)

## Connecting the Logic Analyzer to a System Under Test

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your system under test.

To connect the probes to PPC405GP signals in the system under test using a test clip, follow these steps:

1. Power off your system under test. It is not necessary to power off the logic analyzer.

***CAUTION.*** *To prevent static damage, handle the microprocessor, the probes, and the logic analyzer module only in a static-free environment. Static discharge can damage these components.*

*Always wear a grounding wrist strap, heel strap, or similar device while handling the microprocessor.*

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from the test clip.

***CAUTION.*** *To prevent damage to the pins on the microprocessor,.place the system under test on a horizontal surface before connecting the test clip.*

3. Place the system under test on a horizontal, static-free surface.
4. Use Tables 5–3 through 5–19 beginning on page 5–5 to connect the channel probes to PPC405GP signal pins on the test clip or in the system under test.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

# Operating Basics

# Setting Up the Support

The information in this section is specific to the operations and functions of the TMS 532 PPC405GP microprocessor support on any Tektronix logic analyzer for which it can be purchased.

Before you acquire and display disassembled data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The microprocessor support provides default values for each of these setups as well as user-definable settings.

## Installing the Support Software

***NOTE.*** *Before you install any software, it is recommended you verify that the microprocessor support software is compatible with the logic analyzer software.*

To install the TMS 532 PPC405GP software on your Tektronix logic analyzer, follow these steps:

1. Insert the floppy disk in the disk drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the floppy disk.

To remove or uninstall software, follow the above instructions and select Uninstall. You must close all windows before you uninstall any software.

## Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the TMS 532 PPC405GP support are listed in the following tables:

| 405GPASYNC support | Display radix |
|---|---|
| Address | Hexadecimal |
| Data | Hexadecimal |
| Control | Symbolic |
| ChipSel | OFF |
| ByteEnable | OFF |
| TraceStatus | OFF |
| DMAAck | OFF |

| 405GPSDRAM support | Display radix |
|---|---|
| BusAddr | OFF |
| Address | Hexadecimal |
| Data | Hexadecimal |
| Control | Symbolic |
| BankSelect | OFF |
| Misc | OFF |
| DataMask | OFF |

The channel group tables begin on page 5–1.

## Support Package Setups

The TMS 532 PPC405GP software installs two support package setup files. Each setup file offers different clocking and display options.

### 405GPSDRAM Setup

This setup provides disassembly support for the SDRAM interface. Signals are not inverted and are displayed as they appear electrically on the front side bus.

Disassembly channel groups:

- Sample
- Address
- Data
- Mnemonics
- Control
- Time Stamp

Timing channel groups:

- Control

### 405GPASYNC Setup

This setup provides disassembly support for the Peripheral interface. Signals are not inverted and are displayed as they appear electrically on the front side bus.

Disassembly channel groups:

- Sample
- Address
- Data
- Mnemonics
- Control
- Time Stamp

Timing channel groups:

- Control

# Clocking

## Options

The TMS 532 PPC405GP software offers a microprocessor-specific clocking mode for the PPC405GP microprocessor. This clocking mode is the default selection whenever you load the PPC405GP support.

Disassembly is not correct if you use the Internal or External clocking modes. See your logic analyzer online help for more details on how to use these clock selections for general purpose analysis.

- Internal clocking is used for timing and is based on the clock generated by a Tektronix logic analyzer. You can configure the clock rate from 50 ms down to 4 ns resolution.
- External clocking is used when you configure the clocking of data based on logical combinations of clocks and qualifiers.

## Custom Clocking

When Custom is selected, the Custom Clocking Options menu has the subtitle 405GPSDRAM or 405GPASYNC Microprocessor Clocking Support added, and the clocking options are also displayed.

The TMS 532 PPC405GP supports:

- SDRAM Support
- Peripheral Support

**Setup and Hold Time.** You cannot change the Setup and Hold time for any signal groups.

Figure 2–1 shows an SDRAM timing diagram with default data transitions.

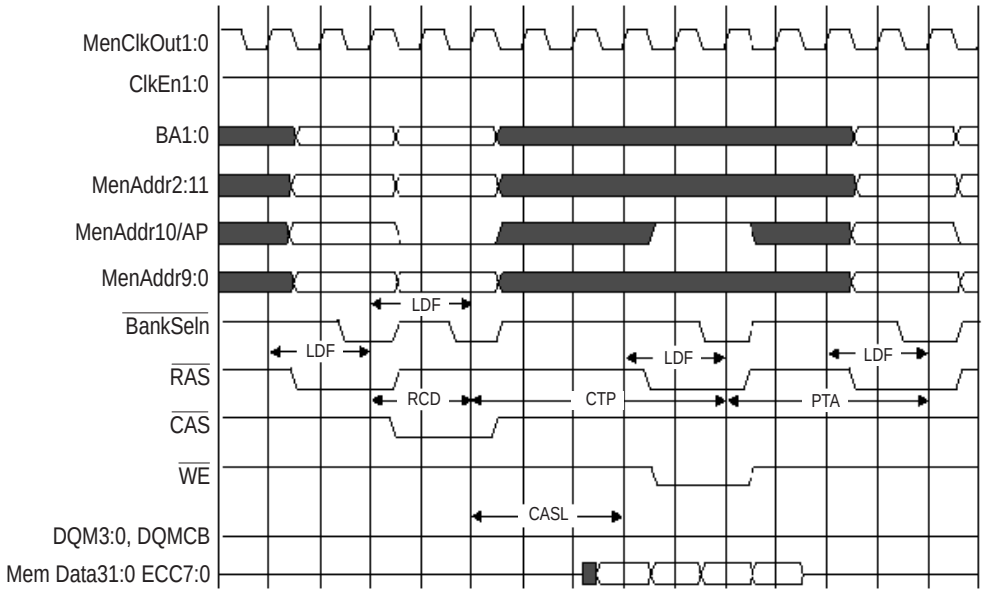


**Figure 2–1: SDRAM timing diagram with activate, four-word read, and percharge cycles**

Figure 2–2 shows an asynchronous memory interface.

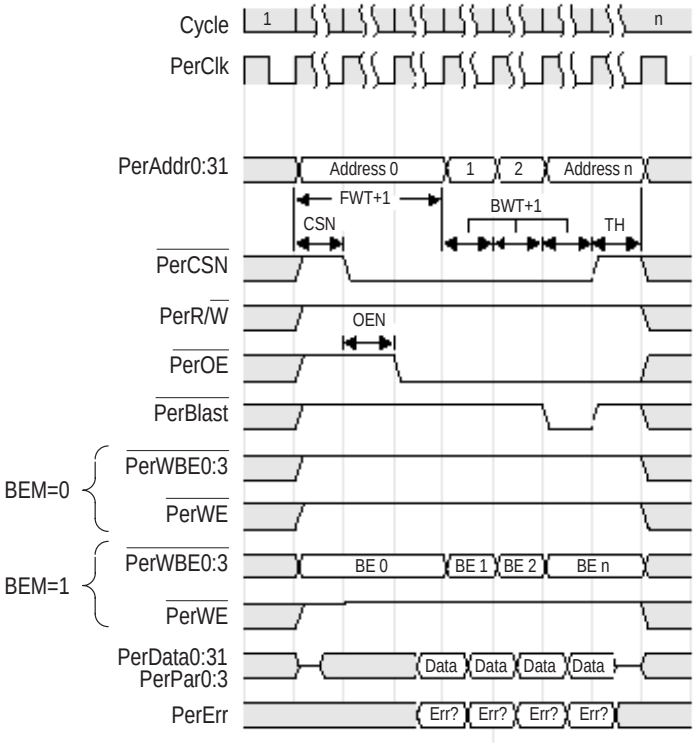


**Figure 2–2: Burst read transfer timing diagram**

# Acquiring and Viewing Disassembled Data

## Acquiring Data

The TMS 532 PPC405GP software package will install 405GPASYNC support for peripheral interface and 405GPSDRAM support for SDRAM Interface.

For viewing peripheral interface disassembly use 405GPASYNC support package and 405GPASYNC channel assignment.

For viewing SDRAM interface disassembly use 405GPSDRAM support package and 405GPSDRAM channel assignment.

Once you load either 405GPASYNC or 405GPSDRAM support packages choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to your logic analyzer online help or *Appendix A: Error Messages and Disassembly Problems* in the user manual.

## Viewing Disassembled Data

You can view disassembled data in six display formats: Timing, State, Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

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***NOTE.*** *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–13.*

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The default display format displays the Address, Data, and Control channel group values for each sample of acquired data.

Any channel group or display column can be made visible by selecting the Add Column option in the Disassembly property page.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–1 lists these special characters and strings and gives a definition of what they represent.

**Table 2–1: Description of special characters in the display**

| Character or string displayed | Definition |
|---|---|
| # | Indicates an immediate value |
| > | Indicates that there is insufficient room on the screen to show all available data. |
| >> | Indicates that the instruction was manually marked. |
| t | Indicates the number shown is in decimal, such as #12t |
| **** | Indicates that there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte. |

If the row address is not acquired for any open page, then the MSB (most significant bit) of the Address column is represented by dashes in the display, and the automatic dequeue is disabled.

- For a Precharge cycle, both the Data and the Address column address are invalidated.
- For a Row address cycle, the Data column is not invalidated for a sequential series of instructions. The disassembler may display "ILLEGAL INSTRUCTION" for multiple word and string reads.

You can not trigger on an address symbol table because the address symbol table is derived from a 13 bit BusAddr group from the 405GPSDRAM setup.

## Timing Display Format

The timing-waveform display format file is provided for logic analyzer support and sets up and displays the following waveforms:

**405GPASYNC**
PerCLK
Address
Data
PerCS0:7
PerR/W~
PerOE~
PerWE~
HoldAck
PerBLast~
PerWBE0:3
ExtAck~
SysReset~
PerReady

**405GPSDRAM**
MemClkOut
Data
BusAddr
BA0
BA1
BankSel 0~:3~
DQM0:3
CAS~
RAS~
WE~
SysReset~
ExtAck~

## Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–2 lists cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors are labeled with the vector name.

**Table 2–2: Cycle type definitions**

| Cycle type | Definition |
|---|---|
| ( FLUSH ) | A cycle was fetched but not executed |
| ( EXTENSION ) | An extension to the preceding instruction opcode |
| ( ALT. BUS MASTER ) | A bus is related to an alternate bus master |
| ( SYSTEM RESET ) | A reset cycle |
| ( REFRESH ) | A refresh cycle |
| ( PRECHARGE ) | A bank precharge cycle |
| ( PRECHARGE ALL ) | Precharge all bank cycle |
| ( ROW ADDRESS ) | Row address |
| ( COLUMN ADDRESS ) | Column address |
| ( DATA WRITE ) | Data write cycle |
| ( DATA READ ) | Data read cycle |
| ( PERIPHERAL ERROR ) | Peripheral error cycle |
| ( ALT.BUS MASTER READ ) | Bus is related to an alternate bus master read |
| ( ALT.BUS MASTER WRITE ) | Bus is related to an alternate bus master write |
| ( DMA READ ) | DMA read cycle |
| ( DMA WRITE ) | DMA write Cycle |
| ( I–CACHE LINE FILL ) | Instruction cache line fill |

Figure 2–3 shows an example of a 405GPSDRAM hardware display.

| Sample | 405GPSDRAM Address | 405GPSDRAM Data | 405GPSDRAM Mnemonics | 405GPSDRAM Control | Timestamp |
|---|---|---|---|---|---|
| 279 | 000301BC | 60210000 | cri r1,r1,Cx0 > | 111:1010111 | 15.000 |
| 281 | 00000C70 | --------- | ( Column Address ) | READ | 135.000 |
| 283 | 000301C0 | 88010003 | lbz r0.0x3(r1) > | 111:1010111 | 30.000 |
| 284 | 000301C4 | 3C600005 | addis r3.0,0x50000 > | 111:1010111 | 15.000 |
| 285 | 000301C8 | 606304A8 | cri r3,r3,Cx4A8 > | 111:1010111 | 15.000 |
| 286 | 000301CC | B0630000 | sth r3,0x0(r3) > | 111:1010111 | 15.000 |
| 288 | --------- | --------- | ( Precharge ) | PRECHARGE | 120.000 |
| 290 | 00000C80 | --------- | ( Row Address ) | ACTIVATE | 30.000 |
| 292 | 00000C00 | --------- | ( Column Address ) | READ | 30.000 |
| 294 | 00040C00 | 00010203 | ( Data Read ) | 111:1010010 | 30.000 |
| 295 | 00040C04 | 04050607 | ( Data Read ) | 111:1010010 | 15.000 |
| 302 | --------- | --------- | ( Precharge ) | PRECHARGE | 105.000 |
| 304 | 00000C60 | --------- | ( Row Address ) | ACTIVATE | 30.000 |
| 306 | 00000C74 | --------- | ( Column Address ) | READ | 30.000 |
| 308 | 000301D0 | 3FE00000 | addis r31.0,Cx00000 > | ACTIVATE | 30.000 |
| 309 | 000301D4 | 63FF0001 | cri r31.r31,0x1 > | 111:1010101 | 15.000 |
| 310 | 000301D8 | 7FE903A6 | mtspr CTR,r31 > | READ | 15.000 |
| 311 | 000301DC | 3FC00000 | addis r30.0,Cx00000 > | 111:1010100 | 15.000 |
| 312 | 00050488 | 00000000 | ( Data Read ) | 111:1010100 | 14.500 |
| 313 | 0005048C | 00000000 | ( Data Read ) | 111:1010100 | 15.500 |
| 316 | 000504A8 | 04A80000 | ( Data Write ) | WRITE | 45.000 |
| 317 | 000504AC | 00000000 | ( Data Write ) | 111:1010111 | 14.500 |
| 320 | 00000C78 | --------- | ( Column Address ) | READ | 45.500 |
| 322 | 000301E0 | 63DE0000 | cri r30.r30,0x0 > | 111:1010111 | 30.000 |
| 323 | 000301E4 | 7FCFF120 | mtcrf 0xFF,r30 > | 111:1010111 | 15.000 |
| 324 | 000301E8 | 40400010 | bc 0x2.0.301F8 > | 111:1010111 | 14.500 |
| 325 | 000301EC | 60000000 | cri r0.r0.Cx0 > | 111:1010111 | 15.000 |
| 327 | 00000C7F | --------- | ( Column Address ) | READ | 135.500 |

**Figure 2–3: 405GPSDRAM hardware display format**

Figure 2–4 shows an example of a 405GPASYNC hardware display.

| Sample | 405GPASYNC Address | 405GPASYNC Data | 405GPASYNC Mnemonics | 405GPASYNC Control | Timestamp |
|---|---|---|---|---|---|
| < 548 | FFF107E8 | 7C------ | wrteei 1 > | BurstRead | 210.000 |
| < 555 | FFF107E9 | 00------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 562 | FFF107EA | 81------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 569 | FFF107EB | 46------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 576 | FFF107EC | 7C------ | xor. r0,r1,r2 > | BurstRead | 210.000 |
| < 583 | FFF107ED | 20------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 590 | FFF107EE | 12------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 597 | FFF107EF | 79------ | ( EXTENSION ) | Single/3> | 210.000 |
| < 603 | FFF107F0 | 7C------ | xor r0,r1,r2 > | BurstRead | 330.000 |
| < 610 | FFF107F1 | 20------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 617 | FFF107F2 | 12------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 624 | FFF107F3 | 78------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 631 | FFF107F4 | 68------ | xori r0,r1,0x3 > | BurstRead | 210.000 |
| < 638 | FFF107F5 | 20------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 645 | FFF107F6 | 00------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 652 | FFF107F7 | 03------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 659 | FFF107F8 | 6C------ | xoris r0,r1,0x30000 > | BurstRead | 209.500 |
| < 666 | FFF107F9 | 20------ | ( EXTENSION ) | BurstRead | 210.500 |
| < 673 | FFF107FA | 00------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 680 | FFF107FB | 03------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 687 | FFF107FC | 4B------ | b FFF10000 > | BurstRead | 209.500 |
| < 694 | FFF107FD | FF------ | ( EXTENSION ) | BurstRead | 210.500 |
| < 701 | FFF107FE | F8------ | ( EXTENSION ) | BurstRead | 210.000 |
| < 708 | FFF107FF | 04------ | ( EXTENSION ) | Single/3> | 210.000 |
| < 714 | FFF10000 | 48------ | b FFF100FC > | BurstRead | 329.500 |

**Figure 2–4: 405GPASYNC hardware display format**

### Software Display Format

The Software display format displays only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions are used to disassemble the instruction, but they are not displayed as a separate cycle in the Software display format. Data reads and writes are not displayed. Figure 2–5 and 2–6 show examples of software displays.

| Sample | 405GPSDRAM Address | 405GPSDRAM Data | 405GPSDRAM Mnemonics | | 405GPSDRAM Control | Timestamp |
|---|---|---|---|---|---|---|
| 606 | D003C230 | A0C50000 | lhz | r6,0x0(r5) | 11111010111 | 165.000 ns |
| 607 | D003C234 | 3C600005 | addis | r3,0,0x50000 | 11111010111 | 15.000 ns |
| 608 | D003C238 | 60630486 | ori | r3,r3,0x486 | 11111010111 | 14.500 ns |
| 609 | D003C23C | 9C630000 | stbu | r3,0x0(r3) | 11111010111 | 15.500 ns |
| 631 | D003C240 | 7ED00400 | mcrxr | crf4 | 11111010101 | 420.000 ns |
| 632 | D003C244 | 7C400026 | mfcr | r2 | 11111010101 | 15.000 ns |
| 633 | D003C248 | 7C500286 | mfdcr | r2,SDRAM0_CFGADDR | READ | 15.000 ns |
| 634 | D003C24C | 7C2000A6 | mfmsr | r1 | 11111010100 | 14.500 ns |
| 645 | D003C250 | 7C0102A6 | mfspr | r0,XER | 11111010111 | 165.000 ns |
| 646 | D003C254 | 7C0C42E6 | mftb | r0,TBL | 11111010111 | 15.000 ns |
| 647 | D003C258 | 3C200005 | addis | r1,0,0x50000 | 11111010111 | 15.000 ns |
| 648 | D003C25C | 6021 04E4 | ori | r1,r1,0x4E4 | 11111010111 | 15.000 ns |
| 652 | D003C260 | 9021 0000 | stw | r1,0x0(r1) | 11111010111 | 165.000 ns |
| 653 | D003C264 | 3E000000 | addis | r16,0,0x00000 | 11111010111 | 15.000 ns |
| 654 | D003C268 | 62100000 | ori | r16,r16,0x0 | 11111010111 | 15.000 ns |
| 655 | D003C26C | 7E005120 | mtcrf | 0x5,r16 | 11111010111 | 15.000 ns |
| 667 | MAT1 | 3C000000 | addis | r0,0,0x00000 | 11111010111 | 285.000 ns |
| 668 | MAT1+4 | 60000000 | ori | r0,r0,0x0 | 11111010111 | 15.500 ns |
| 669 | MAT1+8 | 7C100386 | mtdcr | SDRAM0_CFGADDR,r0 | 11111010111 | 14.500 ns |
| 670 | MAT1+C | 3C200002 | addis | r1,0,0x20000 | 11111010111 | 15.000 ns |
| 674 | MAT1+10 | 6021 9000 | ori | r1,r1,0x9000 | 11111010111 | 165.500 ns |
| 675 | MAT1+14 | 7C200124 | mtmsr | r1 | 11111010111 | 14.500 ns |
| 676 | MAT1+18 | 3C200004 | addis | r1,0,0x40000 | 11111010111 | 15.000 ns |
| 677 | MAT1+1C | 6021 0000 | ori | r1,r1,0x0 | 11111010111 | 15.000 ns |
| 681 | MAT1+20 | 7C01A4AA | lswi | r0,r1,20 | 11111010111 | 165.500 ns |
| 682 | MAT1+24 | 3EC00004 | addis | r22,0,0x40000 | 11111010111 | 15.000 ns |
| 683 | MAT1+28 | 62D60000 | ori | r22,r22,0x0 | 11111010111 | 14.500 ns |
| 684 | MAT1+2C | 3EE00000 | addis | r23,0,0x00000 | 11111010111 | 15.500 ns |
| 7C6 | MAT1+30 | 62F70000 | ori | r23,r23,0x0 | 11111010010 | 419.500 ns |
| 7C7 | MAT1+34 | 7EB6BC2A | lswx | r21,r22,r23 | 11111010010 | 15.000 ns |
| 7C8 | MAT1+38 | 10011151 | mulchw. | r0,r1,r2 | 11111010010 | 15.000 ns |
| 7C9 | MAT1+3C | 10022150 | mulchw | r0,r2,r4 | 11111010010 | 15.000 ns |
| 755 | MAT1+40 | 1253A111 | mulchwu. | r18,r19,r20 | 11111010111 | 915.000 ns |
| 756 | MAT1+44 | 135BE110 | mulchwu | r26,r27,r28 | 11111010111 | 15.000 ns |

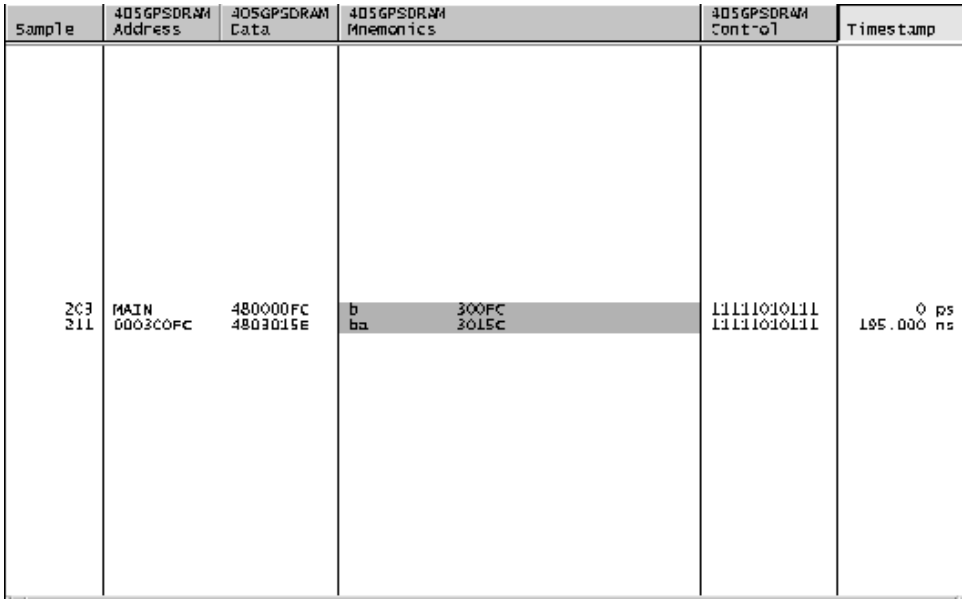
**Figure 2–5: 405GPSDRAM software display format**

| Sample | 405GPASYNC Address | 405GPASYNC Data | 405GPASYNC Mnemonics | | | 405GPASYNC Control | Timestam |
|---|---|---|---|---|---|---|---|
| < 270 | FFF107C0 | 60------ | ori | r5,r5,0x0 | > | BurstRead | 960.000 |
| < 298 | FFF107C4 | 3C------ | addis | r6,0,0x00000 | > | BurstRead | 840.000 |
| < 326 | FFF107C8 | 60------ | ori | r6,r6,0x0 | > | BurstRead | 840.000 |
| < 354 | FFF107CC | 7C------ | tlbsx. | r4,r5,r6 | > | BurstRead | 840.000 |
| < 381 | FFF107D0 | 7C------ | tlbsync | | > | BurstRead | 959.500 |
| < 409 | FFF107D4 | 7C------ | tlbwe | r1,r2,r0 | > | BurstRead | 840.500 |
| < 437 | FFF107D8 | 7C------ | tlbwe | r3,r4,r1 | > | BurstRead | 839.500 |
| < 465 | FFF107DC | 7C------ | tw | 0x0,r1,r2 | > | BurstRead | 840.500 |
| < 492 | FFF107E0 | 0C------ | twi | 0x0,r1,0x30CC | > | BurstRead | 959.500 |
| < 520 | FFF107E4 | 7D------ | wrtee | r8 | > | BurstRead | 840.000 |
| < 548 | FFF107E8 | 7C------ | wrteei | 1 | > | BurstRead | 840.000 |
| < 576 | FFF107EC | 7C------ | xor. | r0,r1,r2 | > | BurstRead | 840.000 |
| < 603 | FFF107F0 | 7C------ | xor | r0,r1,r2 | > | BurstRead | 960.000 |
| < 631 | FFF107F4 | 68------ | xori | r0,r1,0x3 | > | BurstRead | 840.000 |
| < 659 | FFF107F8 | 6C------ | xoris | r0,r1,0x30000 | > | BurstRead | 839.500 |
| < 687 | FFF107FC | 4B------ | b | FFF10000 | > | BurstRead | 840.000 |
| < 714 | FFF10000 | 48------ | b | FFF100FC | > | BurstRead | 960.000 |
| < 853 | FFF100FC | 4B------ | ba | FFF1015C | > | BurstRead | <90,500 |
| < 964 | FFF1015C | 3F------ | addis | r31,0,0x00000 | > | BurstRead | <50,000 |
| < 992 | FFF10150 | 10------ | machhw | r2,r3,r4 | > | BurstRead | 839.500 |
| < 1020 | FFF10154 | 10------ | machhwo. | r3,r4,r5 | > | BurstRead | 840.500 |
| < 1047 | FFF10160 | 63------ | ori | r31,r31,0x1 | > | BurstRead | 929.500 |
| < 1075 | FFF10164 | 7F------ | mtspr | CTR,r31 | > | BurstRead | 840.000 |
| < 1103 | FFF10168 | 42------ | bcl | 0x10,0,FFF1017 | > | BurstRead | 840.000 |
| < 1131 | FFF1016C | 60------ | ori | r0,r0,0x0 | > | BurstRead | 840.000 |

**Figure 2–6: 405GPASYNC software display format**

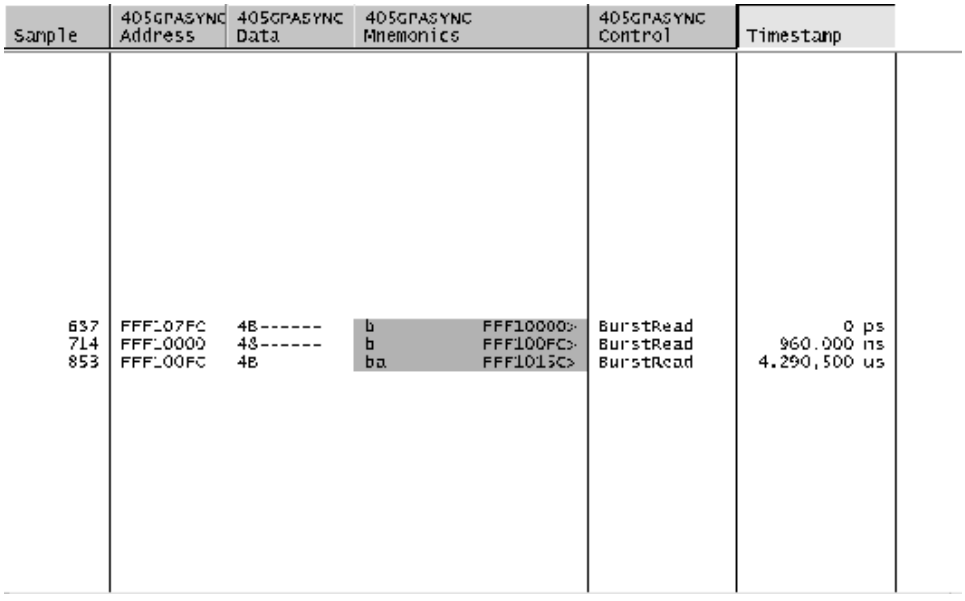
## Control Flow Display Format

The Control Flow display format displays only the first fetch of instructions that cause a branch in the addressing and special cycles to change the flow of control. Figures 2–7 and 2–8 show examples of 405GPSDRAM and 405GPASYNC control flow displays.



| Sample | 405GPSDRAM Address | 405GPSDRAM Data | 405GPSDRAM Mnemonics | | 405GPSDRAM Control | Timestamp |
|---|---|---|---|---|---|---|
| 2C3 | MAIN | 480000FC | b | 300FC | 11111010111 | 0 ps |
| 311 | 0003C0FC | 4803015E | ba | 3015C | 11111010111 | 195.000 ns |

**Figure 2–7: 405GPSDRAM control flow display format**



| Sample | 405GPASYNC Address | 405GPASYNC Data | 405GPASYNC Mnemonics | | 405GPASYNC Control | Timestamp |
|---|---|---|---|---|---|---|
| 637 | FFF107FC | 4B------ | b | FFF10000> | BurstRead | 0 ps |
| 714 | FFF10000 | 4B------ | b | FFF100FC> | BurstRead | 960.000 ns |
| 853 | FFF100FC | 4B | ba | FFF1015C> | BurstRead | 4.290,500 us |

**Figure 2–8: 405GPASYNC control flow display format**

Instructions that generate a change in the flow of control in the PPC405GP microprocessor are as follows:

b target
ba target
bl target
bla target
bc BO, BI, target
bca BO, BI, target
bcl BO, BI, target
bcla BO, BI, target
bcctr BO, BI
bcctrl BO, BI
bclr BO, BI
bclrl BO, BI

### Subroutine Display Format

The Subroutine display format displays only the first fetch of subroutine call and return instructions. It displays conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the PPC405GP microprocessor are as follows:

rfi rfci

## Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

### Optional Display Selections

You can make optional selections for acquired disassembled data. In addition to the common selections (described in your logic analyzer online help), you can change the displayed data in the following ways:

| | | |
|---|---|---|
| Show: | Hardware | (default) |
| | Software | |
| | Control Flow | |
| | Subroutine | |
| Highlight: | Software | (default) |
| | Control Flow | |
| | Subroutine | |
| | None | |
| Disasm Across Gaps: | | Yes (default) |
| | | No |

### Micro-Specific Fields for 405GPASYNC

**Endian Mode.** This field allows you to indicate a PPC405GP processor configuration for viewing data from memory. The following selections are available in the order listed.

True Little Endian
Big Endian (default)

**Exception Prefix.** Enter an EVPR register value in this field.

0000 (default)

**Byte Enable.** Select either Write or Read/Write.

Read/Write (default)
Write

**Bus Width.** The Bus Width field is an 8 bit field and each bit represents a chipselect (CS7, CS6, CS5, CS4, CS3, CS2, CS1, and CS0).

Enter for each chip select signal:
0 for 8 bit bus width
1 for 16 bit bus width
2 for 32 bit bus width

For example, 00000210 in a bus width field indicates that CS2 is connected to a 32 bit device, CS1 is connected to 16 bit device, and CS0 is connected to 8 bit device.

### Micro-Specific Fields 405GPSDRAM

**Endian Mode.** This field allows you to indicate a PPC405GP processor configuration for viewing data from memory. The following selections are available in the order listed.

True Little Endian
Big Endian (default)

**Exception Prefix.** Enter an EVPR register value in this field.

0000 (default)

**CAS~ Latency.** Enter the CAS~ latency of the SDRAM timing register. Enter a number between 2 and 4 (2 is the default).

2 to 4
2 (default)

**SDRAM ADDR Configuration Field.** Table 2–3 lists the common configuration of SDRAM that are fully supported by PPC405GP EMIF. The column, *SDRAM configuration field values*, lists numbers 0x0 through 0xB. Choose one of these numbers for the appropriate SDRAM memory configuration on your board. The default value in the SDRAM ADDR configuration field is 0x0.

***NOTE****. For the IBM PPC405GP Walnut board, the PPC405GP support uses 0x7 in the SDRAM ADDR Configuration Field.*

**Table 2–3: Compatible SDRAM memory configuration**

| Bank size | Organization | SDRAM configuration field values |
|---|---|---|
| 8 MB | 11 * 9 * 2 | 0x0 |
| 16 MB | 11 * 10 * 2 | 0x1 |
| 32 MB | 12 * 9 * 4 | 0x2 |
| 64 MB | 12 * 10 * 4 | 0x3 |
| 64 MB | 13 * 9 * 4 | 0x4 |
| 128 MB | 13 * 11 * 4 | 0x5 |
| 256 MB | 12 * 8 * 2/4 | 0x6 |
| 8/16 MB | 12 * 8 * 2/4 | 0x7 |
| 4/8 MB | 11 * 9 * 2/4 | 0x8 |
| 16/32 MB | 13 * 8 * 2/4 | 0x9 |
| 32 MB | 13 * 9 * 2 | 0xA |
| 64 MB | 13 * 10 * 2 | 0xB |

**Bank0–4 Base Address.** This field contains the bank Base address of the SDRAM Memory configuration register for the base address field.

### Marking Cycles

The TMS 532 PPC405GP support allows you to place marks using the Mark Opcode button. The Mark Opcode is always available. If the sample being marked is not an Address cycle or Data cycle of the potential bus master, the Mark Opcode selections are replaced by a note indicating that “An Opcode Mark cannot be placed at the selected data sample.”

When a cycle is marked, this character, >>, is displayed immediately to the left of the Mnemonics column. Cycles can be unmarked by using the Undo Mark selection, which removes this character. If more than one set of sequences are marked, then the you can undo the marks by using the Remove all Marks option.

The following cycle marks are available:

- Opcode can be marked as Flush
- Flush can be marked as Opcode

## Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided on your PPC405GP software support disk so you can see an example of how your PPC405GP microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your system under test.

# Specifications

# Specifications

This chapter contains information regarding the specifications of the TMS 532 PPC405GP microprocessor support.

## Specification Tables

Tables 3–1 lists the electrical requirements that the system under test must produce for the TMS 532 PPC405GP support to acquire correct data.

**Table 3–1: PPC405GP Electrical specifications**

| Characteristics | Requirements |
|---|---|
| System under test clock rate * | |
| 405GPASYNC Support | |
| Maximum specified clock rate: | 50 MHz |
| Maximum tested clock rate* | 33 MHz |
| Minimum setup time required: 405GPASYNC | 2.5 ns |
| Minimum hold time required: 405GPASYNC | 0 ns |
| 405GPSDRAM Support | |
| Maximum specified clock rate: | 100 MHz |
| Maximum tested clock rate* | 100 MHz |
| Minimum setup time required 405GPSDRAM | 2 ns |
| Minimum hold time required 405GPSDRAM | 0.5 ns |

*** Please contact your Tektronix Sales Representative for current information on the tested clock rate.**

# Replaceable Parts

# Replaceable Parts

This section contains a list of the replaceable parts for the TMS 532 PPC405GP microprocessor support product.

## Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

**Abbreviations**

Abbreviations conform to American National Standard ANSI Y1.1–1972.

**Mfr. Code to Manufacturer Cross Index**

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

## Manufacturers cross index

| Mfr. code | Manufacturer | Address | City, state, zip code |
|---|---|---|---|
| TK2548 | XEROX CORPORATION | 14181 SW MILLIKAN WAY | BEAVERTON, OR 97005 |
| 80009 | TEKTRONIX INC | 14150 SW KARL BRAUN DR<br>PO BOX 500 | BEAVERTON, OR 97077–0001 |

## Replaceable parts list

| Fig. & index number | Tektronix part number | Serial no. effective | Serial no. discont'd | Qty | Name & description | Mfr. code | Mfr. part number |
|---|---|---|---|---|---|---|---|
| | | | | | **STANDARD ACCESSORIES** | | |
| | 071-0892-00 | | | 1 | MANUAL, TECH: INSTRUCTIONS, PPC405GP, TMS532 | TK2548 | 071-0892-00 |
| | | | | | **OPTIONAL ACCESSORIES** | | |
| | P6434* | | | 3 | P6434 MASS TERMINATION PROBE, Opt 21 * | 80009 | ORDER BY DESCRIPTION |

*** Check the P6434 manual for detailed replaceable part information.**

# Reference

# Reference: Tables

This section lists the Symbol table and the Channel group tables for disassembly and timing.

## Symbol Table

Table 5–1 lists the name, bit pattern, and meaning for the symbols in the file 405GPASYNC_Ctrl, the Control channel group symbol table.

**Table 5–1: 405GPASYNC_Cntr group symbol table definitions**

| Symbol | Control group value | | | |
|---|---|---|---|---|
| | SysReset~ | PerErr<br>PerReady<br>HoldAck<br>ExtAck~ | PerR/W~<br>PerBLast~<br>PerOE~<br>PerWE~ | DMAAck0<br>DMAAck1<br>DMAAck2<br>DMAAck3 |
| ResetCycle | 0 | 0 X X X | X X X X | X X X X |
| PeripheralError | X | 1 X X X | X X X X | X X X X |
| Alt.MasterBurstRead | 1 | 0 X 1 0 | 1 1 X X | 0 0 0 0 |
| Alt.MasterBurstWrite | 1 | 0 X 1 0 | 0 1 X X | 0 0 0 0 |
| Alt.MasterSingleRead | 1 | 0 X 1 0 | 1 0 X X | 0 0 0 0 |
| Alt.MasterSingleWrite | 1 | 0 X 1 0 | 0 0 X X | 0 0 0 0 |
| Device–PacedSingleRead | 1 | 0 1 X X | 1 0 0 1 | 0 0 0 0 |
| Device–PacedSingleWrite | 1 | 0 1 X X | 0 0 1 0 | 0 0 0 0 |
| Device–PacedBurstRead | 1 | 0 1 X X | 1 1 0 1 | 0 0 0 0 |
| Device–PacedBurstWrite | 1 | 0 1 X X | 0 1 1 1 | 0 0 0 0 |
| Single/BurstReadEnd | 1 | 0 0 0 1 | 1 0 0 1 | 0 0 0 0 |
| Single/BurstWriteEnd | 1 | 0 0 0 1 | 0 0 1 0 | 0 0 0 0 |
| BurstRead | 1 | 0 0 0 1 | 1 1 0 1 | 0 0 0 0 |
| BurstWrite | 1 | 0 0 0 1 | 0 1 1 0 | 0 0 0 0 |
| DMAWrite | 1 | 0 X X X | 0 X X X | 1 X X X<br>X 1 X X<br>X X 1 X<br>X X X 1 |
| DMARead | 1 | 0 X X X | 1 X X X | 1 X X X<br>X 1 X X<br>X X 1 X<br>X X X 1 |

**Table 5–2: 405GPSDRAM_Cntr group symbol table definitions**

| Symbol | Control group value | | | |
|---|---|---|---|---|
| | SysReset~ | BankSelet3~ BankSelet2~ BankSelet1~ | BankSelet0~ HoldAck ExtAck~ D1:2 (A10)/(AP) | RAS~ CAS~ WE~ |
| RESET | 0 | X X X | X X X X | X X X |
| READ | 1 | X X X | 0 0 1 0 | 1 0 1 |
| READ | 1 | X X 0 | X 0 1 0 | 1 0 1 |
| READ | 1 | X 0 X | X 0 1 0 | 1 0 1 |
| READ | 1 | 0 X X | X 0 1 0 | 1 0 1 |
| READ&AUTOPRECHARGE | 1 | X X X | 0 0 1 1 | 1 0 1 |
| READ&AUTOPRECHARGE | 1 | X X 0 | X 0 1 1 | 1 0 1 |
| READ&AUTOPRECHARGE | 1 | X 0 X | X 0 1 1 | 1 0 1 |
| READ&AUTOPRECHARGE | 1 | 0 X X | X 0 1 1 | 1 0 1 |
| WRITE | 1 | X X X | 0 0 1 0 | 1 0 0 |
| WRITE | 1 | X X 0 | X 0 1 0 | 1 0 0 |
| WRITE | 1 | X 0 X | X 0 1 0 | 1 0 0 |
| WRITE | 1 | 0 X X | X 0 1 0 | 1 0 0 |
| WRITE&AUTOPRECHARGE | 1 | X X X | 0 0 1 1 | 1 0 0 |
| WRITE&AUTOPRECHARGE | 1 | X X 0 | X 0 1 1 | 1 0 0 |
| WRITE&AUTOPRECHARGE | 1 | X 0 X | X 0 1 1 | 1 0 0 |
| WRITE&AUTOPRECHARGE | 1 | 0 X X | X 0 1 1 | 1 0 0 |
| ACTIVATE | 1 | X X X | 0 0 1 X | 0 1 1 |
| ACTIVATE | 1 | X X 0 | X 0 1 X | 0 1 1 |
| ACTIVATE | 1 | X 0 X | X 0 1 X | 0 1 1 |
| ACTIVATE | 1 | 0 X X | X 0 1 X | 0 1 1 |
| PRECHARGE | 1 | X X X | 0 0 1 0 | 0 1 0 |
| PRECHARGE | 1 | X X 0 | X 0 1 0 | 0 1 0 |
| PRECHARGE | 1 | X 0 X | X 0 1 0 | 0 1 0 |
| PRECHARGE | 1 | 0 X X | X 0 1 0 | 0 1 0 |
| PRECHARGE_ALL | 1 | X X X | 0 0 1 1 | 0 1 0 |
| PRECHARGE_ALL | 1 | X X 0 | X 0 1 1 | 0 1 0 |
| PRECHARGE_ALL | 1 | X 0 X | X 0 1 1 | 0 1 0 |
| PRECHARGE_ALL | 1 | 0 X X | X 0 1 1 | 0 1 0 |
| REFRESH | 1 | X X X | 0 0 1 X | 0 0 1 |
| REFRESH | 1 | X X 0 | X 0 1 X | 0 0 1 |

**Table 5–2: 405GPSDRAM_Cntr group symbol table definitions (cont.)**

| Symbol | Control group value | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SysReset~ | | | BankSelet3~ | BankSelet2~ | BankSelet1~ | | | BankSelet0~ | HoldAck | ExtAck~ | | | D1:2 (A10)/(AP) | | | RAS~ | CAS~ | WE~ | | | | |
| REFRESH | 1 | | | X | 0 | X | | | X | 0 | 1 | X | | | | | 0 | 0 | 1 | | | | |
| REFRESH | 1 | | | 0 | X | X | | | X | 0 | 1 | X | | | | | 0 | 0 | 1 | | | | |

## Channel Assignments

Channel assignments listed in Tables 5–3 through 5–19 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are listed starting with the most significant bit (MSB), descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde symbol (~) following a signal name indicates an active low signal.
- An equals symbol (=) following a signal name indicates that it is double probed.
- The module in the lower-numbered slot is referred to as the Master module and the module in the higher-numbered slot is referred to as the Slave module.

  The portable logic analyzer has the lower-numbered slots on the top, and the benchtop logic analyzer has the lower-numbered slots on the left.

**405GPASYNC Support.** The channel assignment groups are displayed in the following order:

| Group name | Display radix |
|---|---|
| Address | Hexadecimal |
| Data | Hexadecimal |
| Mnemonic | None |
| Control | Symbolic |
| Chip select | Off |
| Byte Enable | Off |
| Trace Status | Off |
| DMAAck | Off |

**405GPSDRAM Support.** The channel assignment groups are displayed in the following order:

| Group name | Display radix |
|---|---|
| BUSAddr | Hexadecimal |
| Data | Hexadecimal |
| Mnemonic | None |
| Control | Symbolic |
| BankSelect | Off |
| Misc | Off |
| DataMask | Off |

Table 5–3 lists the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, the Data channel group assignments are displayed in hexadecimal.

**Table 5–3: Address channel group assignments for 405GPASYNC**

| Bit order | Section:channel | 405GPASYNC signal name |
|---|---|---|
| 31 | A3:7 | PerAddr0 |
| 30 | A3:6 | PerAddr1 |
| 29 | A3:5 | PerAddr2 |
| 28 | A3:4 | PerAddr3 |
| 27 | A3:3 | PerAddr4 |
| 26 | A3:2 | PerAddr5 |
| 25 | A3:1 | PerAddr6 |
| 24 | A3:0 | PerAddr7 |
| 23 | A2:7 | PerAddr8 |
| 22 | A2:6 | PerAddr9 |
| 21 | A2:5 | PerAddr10 |
| 20 | A2:4 | PerAddr11 |
| 19 | A2:3 | PerAddr12 |
| 18 | A2:2 | PerAddr13 |
| 17 | A2:1 | PerAddr14 |
| 16 | A2:0 | PerAddr15 |
| 15 | A1:7 | PerAddr16 |
| 14 | A1:6 | PerAddr17 |
| 13 | A1:5 | PerAddr18 |
| 12 | A1:4 | PerAddr19 |
| 11 | A1:3 | PerAddr20 |
| 10 | A1:2 | PerAddr21 |
| 9 | A1:1 | PerAddr22 |
| 8 | A1:0 | PerAddr23 |
| 7 | A0:7 | PerAddr24 |
| 6 | A0:6 | PerAddr25 |
| 5 | A0:5 | PerAddr26 |
| 4 | A0:4 | PerAddr27 |

**Table 5–3: Address channel group assignments for 405GPASYNC (cont.)**

| Bit order | Section:channel | 405GPASYNC signal name |
|---|---|---|
| 3 | A0:3 | PerAddr28 |
| 2 | A0:2 | PerAddr29 |
| 1 | A0:1 | PerAddr30 |
| 0 | A0:0 | PerAddr31 |

Table 5–4 lists the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, the Data channel group assignments are displayed in hexadecimal.

**Table 5–4: Data channel group assignments for 405GPASYNC**

| Bit order | Section:channel | 405GPASYNC signal name |
|---|---|---|
| 31 | D3:7 | PerData0 |
| 30 | D3:6 | PerData1 |
| 29 | D3:5 | PerData2 |
| 28 | D3:4 | PerData3 |
| 27 | D3:3 | PerData4 |
| 26 | D3:2 | PerData5 |
| 25 | D3:1 | PerData6 |
| 24 | D3:0 | PerData7 |
| 23 | D2:7 | PerData8 |
| 22 | D2:6 | PerData9 |
| 21 | D2:5 | PerData10 |
| 20 | D2:4 | PerData11 |
| 19 | D2:3 | PerData12 |
| 18 | D2:2 | PerData13 |
| 17 | D2:1 | PerData14 |
| 16 | D2:0 | PerData15 |
| 15 | D1:7 | PerData16 |
| 14 | D1:6 | PerData17 |
| 13 | D1:5 | PerData18 |
| 12 | D1:4 | PerData19 |
| 11 | D1:3 | PerData20 |
| 10 | D1:2 | PerData21 |

**Table 5–4: Data channel group assignments for 405GPASYNC (cont.)**

| Bit order | Section:channel | 405GPASYNC signal name |
|---|---|---|
| 9 | D1:1 | PerData22 |
| 8 | D1:0 | PerData23 |
| 7 | D0:7 | PerData24 |
| 6 | D0:6 | PerData25 |
| 5 | D0:5 | PerData26 |
| 4 | D0:4 | PerData27 |
| 3 | D0:3 | PerData28 |
| 2 | D0:2 | PerData29 |
| 1 | D0:1 | PerData30 |
| 0 | D0:0 | PerData31 |

Table 5–5 lists the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. The default radix of the Control group is SYMBOLIC on the logic analyzer. The symbol table file name is 405GPASYNC_Ctrl on the logic analyzer.

**Table 5–5: Control channel group assignments for 405GPASYNC**

| Bit order | Section:channel | 405GPASYNC signal name |
|---|---|---|
| 11 | C2:1 | SysReset~ |
| 10 | C1:3 | PerErr |
| 9 | Q1 | PerReady |
| 8 | C1:2 | HoldAck |
| 7 | CLK0 | PerR/W~ |
| 6 | CLK3 | PerBLast~ |
| 5 | C2:0 | PerOE~ |
| 4 | C2:3 | PerWE~ |
| 3 | C2:7 | DMAAck0 |
| 2 | C2:6 | DMAAck1 |
| 1 | C2:5 | DMAAck2 |
| 0 | C2:4 | DMAAck3 |

The Chip Select channel group assignments shown in Table 5–6 are not displayed by default.

**Table 5–6: Chip Select channel group assignments for 405GPASYNC**

| Bit order | Section:channel | 405GPASYNC signal name |
|---|---|---|
| 7 | C0:7 | PerCS0 |
| 6 | C0:6 | PerCS1 |
| 5 | C0:5 | PerCS2 |
| 4 | C0:4 | PerCS3 |
| 3 | C0:3 | PerCS4 |
| 2 | C0:2 | PerCS5 |
| 1 | C0:1 | PerCS6 |
| 0 | C0:0 | PerCS7 |

The Byte Enable channel group assignments shown in Table 5–7 are not displayed by default.

**Table 5–7: Byte Enable channel group assignments for 405GPASYNC**

| Bit order | Section:channel | 405GPASYNC signal name |
|---|---|---|
| 3 | C1:7 | PerWBE0~ |
| 2 | C1:6 | PerWBE1~ |
| 1 | C1:5 | PerWBE2~ |
| 0 | C1:4 | PerWBE3~ |

The Trace Status channel group assignments shown in Table 5–8 are not displayed.

**Table 5–8: Trace Status channel group assignments for 405GPASYNC**

| Bit order | Section:channel | 405GPASYNC signal name |
|---|---|---|
| 7 | C3:7 | TS1O |
| 6 | C3:6 | TS1E |
| 5 | C3:5 | TS2O |
| 4 | C3:4 | TS2E |

**Table 5–8: Trace Status channel group assignments for 405GPASYNC (cont.)**

| Bit order | Section:channel | 405GPASYNC signal name |
|---|---|---|
| 3 | C3:3 | TS3 |
| 2 | C3:2 | TS4 |
| 1 | C3:1 | TS5 |
| 0 | C3:0 | TS6 |

The DMA Acknowledge channel group assignments shown in Table 5–9 are not displayed by default.

**Table 5–9: DMA Acknowledge channel group assignments for 405GPASYNC**

| Bit order | Section:channel | 405GPASYNC signal name |
|---|---|---|
| 3 | C2:7 | DMAAck0 |
| 2 | C2:6 | DMAAck1 |
| 1 | C2:5 | DMAAck2 |
| 0 | C2:4 | DMAAck3 |

Table 5–10 lists the probe section and clock and qualifier channel assignments. The clock probes are not part of any group.

**Table 5–10: Clock and Qualifier channel assignments for 405GPASYNC**

| Section:channel | 405GPASYNC signal name |
|---|---|
| CLK:0 | PerR/W~ |
| CLK:1 | PerClk |
| CLK:3 | PerBLast~ |
| C2:0 | PerOE~ |
| C2:1 | SysReset~ |
| C2:2 | ExtAck~ |
| C2:3 | PerWE~ |
| QUAL:1 | PerReady |

**Acquisition Setup.** The TMS 532 PPC405GP support affects the logic analyzer setup menus (and submenus) by modifying existing fields and adding micro-specific fields.

The TMS 532 PPC405GP support adds the selection 405GPASYNC and 405GPSDRAM to the Load Support Package dialog box, under the File pulldown menu. Once the 405GPASYNC and 405GPSDRAM supports are loaded, the Custom clocking mode selection in the module Setup menu is also enabled.

Table 5–11 lists the 405GPASYNC signals required for clocking and disassembly.

**Table 5–11: 405GPASYNC signals required for clocking and disassembly**

| Channel name | PPC405GP signal name |
|---|---|
| PerAddr31–0 | A3:0–7 |
| (Address Group) | A2:0–7 |
| – | A1:0–7 |
| – | A0:0–7 |
| – | – |
| PerData31–0 | D3:0–7 |
| (Data Group) | D2:0–7 |
| – | D1:0–7 |
| – | D0:0–7 |
| CLK0 | PerR/W~ |
| CLK1 | PerClk |
| CLK3 | PerBLast~ |
| Q1 | PerReady |
| C0:7 | PerCS0 |
| C0:6 | PerCS1 |
| C0:5 | PerCS2 |
| C0:4 | PerCS3 |
| C0:3 | PerCS4 |
| C0:2 | PerCS5 |
| C0:1 | PerCS6 |
| C0:0 | PerCS7 |
| C1:2 | HoldAck |
| C1:3 | PerErr |

**Table 5–11: 405GPASYNC signals required for clocking and disassembly (cont.)**

| Channel name | PPC405GP signal name |
|---|---|
| C1:4 | PerWBE3~ |
| C1:5 | PerWBE2~ |
| C1:6 | PerWBE1~ |
| C1:7 | PerWBE0~ |
| C2:0 | PerOE~ |
| C2:1 | SysReset~ |
| C2:2 | ExtAck~ |
| C2:3 | PerWE~ |
| C2:4 | DMAAck3 |
| C2:5 | DMAAck2 |
| C2:6 | DMAAck1 |
| C2:7 | DMAAck0 |

Table 5–12 lists the 405GPASYNC signals not required for clocking and disassembly.

**Table 5–12: 405GPASYNC signals not required for clocking and disassembly**

| Channel name | 405GPASYNC signal name |
|---|---|
| C3:7 | TS1O |
| C3:6 | TS1E |
| C3:5 | TS2O |
| C3:4 | TS2E |
| C3:3 | TS3 |
| C3:2 | TS4 |
| C3:1 | TS5 |
| C3:0 | TS6 |

## 405GPSDRAM Channel Group Assignments

Table 5–13 lists the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, the Address channel group assignments are displayed in hexadecimal.

**Table 5–13: TLA Group A channel assignments for 405GPSDRAM**

| Bit order | Channel name | 405GPSDRAM signal name |
|---|---|---|
| 0 | A3:7 | MemData0 |
| 1 | A3:6 | MemData1 |
| 2 | A3:5 | MemData2 |
| 3 | A3:4 | MemData3 |
| 4 | A3:3 | MemData4 |
| 5 | A3:2 | MemData5 |
| 6 | A3:1 | MemData6 |
| 7 | A3:0 | MemData7 |
| 8 | A2:7 | MemData8 |
| 9 | A2:6 | MemData9 |
| 10 | A2:5 | MemData10 |
| 11 | A2:4 | MemData11 |
| 12 | A2:3 | MemData12 |
| 13 | A2:2 | MemData13 |
| 14 | A2:1 | MemData14 |
| 15 | A2:0 | MemData15 |
| 16 | A1:7 | MemData16 |
| 17 | A1:6 | MemData17 |
| 18 | A1:5 | MemData18 |
| 19 | A1:4 | MemData19 |
| 20 | A1:3 | MemData20 |
| 21 | A1:2 | MemData21 |
| 22 | A1:1 | MemData22 |
| 23 | A1:0 | MemData23 |
| 24 | A0:7 | MemData24 |
| 25 | A0:6 | MemData25 |
| 26 | A0:5 | MemData26 |
| 27 | A0:4 | MemData27 |
| 28 | A0:3 | MemData28 |

**Table 5–13: TLA Group A channel assignments for 405GPSDRAM (cont.)**

| Bit order | Channel name | 405GPSDRAM signal name |
|---|---|---|
| 29 | A0:2 | MemData29 |
| 30 | A0:1 | MemData30 |
| 31 | A0:0 | MemData31 |

Table 5–14 lists the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, the Data channel group assignments are displayed in hexadecimal.

**Table 5–14: TLA group D channel assignments for 405GPSDRAM**

| Bit order | Channel name | 405GPSDRAM signal name |
|---|---|---|
| 12 | D0:0 | MemAddr0 |
| 11 | D0:1 | MemAddr1 |
| 10 | D0:2 | MemAddr2 |
| 9 | D0:3 | MemAddr3 |
| 8 | D0:4 | MemAddr4 |
| 7 | D0:5 | MemAddr5 |
| 6 | D0:6 | MemAddr6 |
| 5 | D0:7 | MemAddr7 |
| 4 | D1:0 | MemAddr8 |
| 3 | D1:1 | MemAddr9 |
| 2 | D1:2 | MemAddr10 |
| 1 | D1:3 | MemAddr11 |
| 0 | D1:4 | MemAddr12 |

Table 5–15 lists the probe section and clock and qualifier channel assignments. The clock probes are not part of any group.

**Table 5–15: Clock and Qualifier channel assignments for 405GPSDRAM**

| Channel name | 405GPSDRAM signal name | Comments | |
|---|---|---|---|
| CLK:3 | MemClkOut0 | – | CLK |
| C2:0 | RAS~ | RowAddressStrobe | Qual |
| C2:1 | CAS~ | ColoumAddressStrobe | Qual |
| C2:2 | WE~ | WriteEnable | Qual |

Table 5–16 lists the Bank Select channel assignments. By default, this channel group is not displayed.

**Table 5–16: Bank Select channel assignments for 405GPSDRAM**

| Bit order | Channel name | 405GPSDRAM signal name |
|---|---|---|
| 3 | C3:0 | BankSel3~ |
| 2 | C3:1 | BankSel2~ |
| 1 | C3:2 | BankSel1~ |
| 0 | C3:3 | BankSel0~ |

Table 5–17 lists the Bank Access channel assignments. By default, this channel group is not displayed.

**Table 5–17: Bank Access channel assignments for 405GPSDRAM**

| Bit order | Channel name | 405GPSDRAM signal name |
|---|---|---|
| 1 | D1:6 | BA0 |
| 0 | D1:7 | BA1 |

Table 5–18 lists the Data Mask channel assignments. By default, this channel group is not displayed.

**Table 5–18: Data Mask channel assignments for 405GPSDRAM**

| Bit order | Channel name | 405GPSDRAM signal name |
|---|---|---|
| 3 | C2:4 | DQM3 |
| 2 | C2:5 | DQM2 |
| 1 | C2:6 | DQM1 |
| 0 | C2:7 | DQM0 |

Table 5–19 All signals are required for clocking and disassembly for the 405GPSDRAM interface.

**Table 5–19: Signals required for clocking and disassembly for 405GPSDRAM**

| Channel name | 405GPSDRAM signal name |
|---|---|
| MemAddr12–0 | D0:7–0 |
| (Address Group) | D1:4–0 |
| MemData31:0 | A3:0–7 |
| (Data Group) | A2:0–7 |
| – | A1:0–7 |
| – | A0:0–7 |
| CLK:0 | SysReset~ |
| CLK:2 | ExtAck~ |
| CLK:3 | MemClkOut0 |
| C3:0 | BankSel3~ |
| C3:1 | BankSel2~ |
| C3:2 | BankSel1~ |
| C3:3 | BankSel0~ |
| C2:2 | WE~ |
| C2:1 | CAS~ |
| C2:0 | RAS~ |

**Table 5–19: Signals required for clocking and disassembly for 405GPSDRAM (cont.)**

| Channel name | 405GPSDRAM signal name |
|---|---|
| D1:6 | BA0 |
| D1:7 | BA1 |
| C2:7 | DQM0 |
| C2:6 | DQM1 |
| C2:5 | DQM2 |
| C2:4 | DQM3 |
| C2:3 | HoldAck |

## CPU To Mictor Connections

To probe the microprocessor you need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the *P6434 Mass Termination Probe* manual, Tektronix part number 070-9793-xx, for more information on mechanical specifications. Tables 5–20 through 5–24 list the CPU pin to Mictor pin connections.

Tektronix uses a counterclockwise pin assignment. Pin 1 is located at the top left, and pin 2 is located directly below it. Pin 20 is located on the bottom right, and pin 21 is located directly above it.

AMP uses an odd side even side pin assignment. Pin 1 is located at the top left, and pin 3 is located directly below it. Pin 2 is located on the top right, and pin 4 is located directly below it (see Figure 5–1).

***NOTE.*** *When designing Mictor connectors into your system under test, always follow the Tektronix pin assignment.*

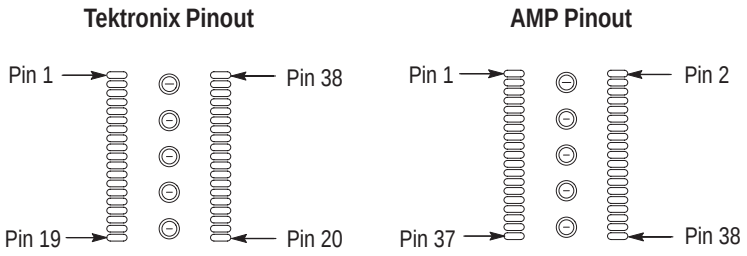



**Figure 5–1: Pin assignments for a Mictor connector (component side)**

***CAUTION.*** *To protect the CPU and the inputs of the module, it is recommended that a 180 Ω resistor is connected in series between each ball pad of the CPU and each pin of the Mictor connector. The resistor must be within 1/2 inch of the ball pad of the CPU.*

## 405GPASYNC Mictor Connections

Tables 5–20 through 5–22 list the microprocessor signals visible at the mictor connectors.

**Table 5–20: CPU to Mictor connections for Mictor A pins for 405GPASYNC**

| Tektronix Mictor A pin number | AMP Mictor A pin number | Logic analyzer channel | 405GPASYNC signal name | Comments |
|---|---|---|---|---|
| 01 | 01 | – | – | Not Connected |
| 02 | 03 | – | – | Not Connected |
| 03 | 05 | Clock 0 | PerR/W~ | Read/Write |
| 04 | 07 | A3:7 | Addr 0 | ASYNC Address |
| 05 | 09 | A3:6 | Addr 1 | ASYNC Address |
| 06 | 11 | A3:5 | Addr 2 | ASYNC Address |
| 07 | 13 | A3:4 | Addr 3 | ASYNC Address |
| 08 | 15 | A3:3 | Addr 4 | ASYNC Address |
| 09 | 17 | A3:2 | Addr 5 | ASYNC Address |
| 10 | 19 | A3:1 | Addr 6 | ASYNC Address |
| 11 | 21 | A3:0 | Addr 7 | ASYNC Address |
| 12 | 23 | A2:7 | Addr 8 | ASYNC Address |
| 13 | 25 | A2:6 | Addr 9 | ASYNC Address |
| 14 | 27 | A2:5 | Addr 10 | ASYNC Address |
| 15 | 29 | A2:4 | Addr 11 | ASYNC Address |
| 16 | 31 | A2:3 | Addr 12 | ASYNC Address |
| 17 | 33 | A2:2 | Addr 13 | ASYNC Address |
| 18 | 35 | A2:1 | Addr 14 | ASYNC Address |
| 19 | 37 | A2:0 | Addr 15 | ASYNC Address |
| 20 | 38 | A0:0 | Addr 31 | ASYNC Address |
| 21 | 36 | A0:1 | Addr 30 | ASYNC Address |
| 22 | 34 | A0:2 | Addr 29 | ASYNC Address |
| 23 | 32 | A0:3 | Addr 28 | ASYNC Address |
| 24 | 30 | A0:4 | Addr 27 | ASYNC Address |
| 25 | 28 | A0:5 | Addr 26 | ASYNC Address |
| 26 | 26 | A0:6 | Addr 25 | ASYNC Address |
| 27 | 24 | A0:7 | Addr 24 | ASYNC Address |
| 28 | 22 | A1:0 | Addr 23 | ASYNC Address |

**Table 5–20: CPU to Mictor connections for Mictor A pins for 405GPASYNC (cont.)**

| Tektronix Mictor A pin number | AMP Mictor A pin number | Logic analyzer channel | 405GPASYNC signal name | Comments |
|---|---|---|---|---|
| 29 | 20 | A1:1 | Addr 22 | ASYNC Address |
| 30 | 18 | A1:2 | Addr 21 | ASYNC Address |
| 31 | 16 | A1:3 | Addr 20 | ASYNC Address |
| 32 | 14 | A1:4 | Addr 19 | ASYNC Address |
| 33 | 12 | A1:5 | Addr 18 | ASYNC Address |
| 34 | 10 | A1:6 | Addr 17 | ASYNC Address |
| 35 | 08 | A1:7 | Addr 16 | ASYNC Address |
| 36 | 06 | Clock 1 | PerClk | ASYNC Clock |

**Table 5–21: CPU to Mictor connections for Mictor C pins for 405GPASYNC**

| Tektronix Mictor C pin number | AMP Mictor C pin number | LA channel | 405GPASYNC signal name | Comments |
|---|---|---|---|---|
| 03 | 05 | Clock 3 | PerBLast~ | Burst Last |
| 04 | 07 | C3:7 | TS1O | Trace Status |
| 05 | 09 | C3:6 | TS1E | Trace Status |
| 06 | 11 | C3:5 | TS2O | Trace Status |
| 07 | 13 | C3:4 | TS2E | Trace Status |
| 08 | 15 | C3:3 | TS3 | Trace Status |
| 09 | 17 | C3:2 | TS4 | Trace Status |
| 10 | 19 | C3:1 | TS5 | Trace Status |
| 11 | 21 | C3:0 | TS6 | Trace Status |
| 12 | 23 | C2:7 | DMAAck0 | DMA Acknowledge |
| 13 | 25 | C2:6 | DMAAck1 | DMA Acknowledge |
| 14 | 27 | C2:5 | DMAAck2 | DMA Acknowledge |
| 15 | 29 | C2:4 | DMAAck3 | DMA Acknowledge |
| 16 | 31 | C2:3 | PerWE~ | ASYNC Write Enable |
| 17 | 33 | C2:2 | ExtAck~ | External Acknowledge |
| 18 | 35 | C2:1 | SysReset~ | System Reset |

**Table 5–21: CPU to Mictor connections for Mictor C pins for 405GPASYNC (cont.)**

| Tektronix Mictor C pin number | AMP Mictor C pin number | LA channel | 405GPASYNC signal name | Comments |
|---|---|---|---|---|
| 19 | 37 | C2:0 | PerOE~ | ASYNC Output Enable |
| 20 | 38 | C0:0 | PerCS7 | Chip Select |
| 21 | 36 | C0:1 | PerCS6 | Chip Select |
| 22 | 34 | C0:2 | PerCS5 | Chip Select |
| 23 | 32 | C0:3 | PerCS4 | Chip Select |
| 24 | 30 | C0:4 | PerCS3 | Chip Select |
| 25 | 28 | C0:5 | PerCS2 | Chip Select |
| 26 | 26 | C0:6 | PerCS1 | Chip Select |
| 27 | 24 | C0:7 | PerCS0 | Chip Select |
| 28 | 22 | C1:0 | – | – |
| 29 | 20 | C1:1 | – | – |
| 30 | 18 | C1:2 | HoldAck | Hold Acknowledge |
| 31 | 16 | C1:3 | PerErr | ASYNC Error |
| 32 | 14 | C1:4 | PerWBE3~ | ASYNC WriteByteEnable |
| 33 | 12 | C1:5 | PerWBE2~ | ASYNC WriteByteEnable |
| 34 | 10 | C1:6 | PerWBE1~ | ASYNC WriteByteEnable |
| 35 | 08 | C1:7 | PerWBE0~ | ASYNC WriteByteEnable |
| 36 | 06 | Qual 1 | PerReady | ASYNC Ready |
| 37 | 04 | – | – | Not Connected |
| 38 | 02 | – | – | Not Connected |

**Table 5–22: CPU to Mictor connections for Mictor D pins for 405GPASYNC**

| Tektronix Mictor D pin number | AMP Mictor D pin number | LA channel | 405GPASYNC signal name | Comments |
|---|---|---|---|---|
| 01 | 01 | – | – | Not Connected |
| 02 | 03 | – | – | Not Connected |
| 03 | 05 | – | – | Not Connected |

**Table 5–22: CPU to Mictor connections for Mictor D pins for 405GPASYNC (cont.)**

| Tektronix Mictor D pin number | AMP Mictor D pin number | LA channel | 405GPASYNC signal name | Comments |
|---|---|---|---|---|
| 04 | 07 | D3:7 | PerData 0 | Peripheral Data |
| 05 | 09 | D3:6 | PerData 1 | Peripheral Data |
| 06 | 11 | D3:5 | PerData 2 | Peripheral Data |
| 07 | 13 | D3:4 | PerData 3 | Peripheral Data |
| 08 | 15 | D3:3 | PerData 4 | Peripheral Data |
| 09 | 17 | D3:2 | PerData 5 | Peripheral Data |
| 10 | 19 | D3:1 | PerData 6 | Peripheral Data |
| 11 | 21 | D3:0 | PerData 7 | Peripheral Data |
| 12 | 23 | D2:7 | PerData 8 | Peripheral Data |
| 13 | 25 | D2:6 | PerData 9 | Peripheral Data |
| 14 | 27 | D2:5 | PerData 10 | Peripheral Data |
| 15 | 29 | D2:4 | PerData 11 | Peripheral Data |
| 16 | 31 | D2:3 | PerData 12 | Peripheral Data |
| 17 | 33 | D2:2 | PerData 13 | Peripheral Data |
| 18 | 35 | D2:1 | PerData 14 | Peripheral Data |
| 19 | 37 | D2:0 | PerData 15 | Peripheral Data |
| 20 | 38 | D0:0 | PerData 31 | Peripheral Data |
| 21 | 36 | D0:1 | PerData 30 | Peripheral Data |
| 22 | 34 | D0:2 | PerData 29 | Peripheral Data |
| 23 | 32 | D0:3 | PerData 28 | Peripheral Data |
| 24 | 30 | D0:4 | PerData 27 | Peripheral Data |
| 25 | 28 | D0:5 | PerData 26 | Peripheral Data |
| 26 | 26 | D0:6 | PerData 25 | Peripheral Data |
| 27 | 24 | D0:7 | PerData 24 | Peripheral Data |
| 28 | 22 | D1:0 | PerData 23 | Peripheral Data |
| 29 | 20 | D1:1 | PerData 22 | Peripheral Data |
| 30 | 18 | D1:2 | PerData 21 | Peripheral Data |
| 31 | 16 | D1:3 | PerData 20 | Peripheral Data |
| 32 | 14 | D1:4 | PerData 19 | Peripheral Data |
| 33 | 12 | D1:5 | PerData 18 | Peripheral Data |
| 34 | 10 | D1:6 | PerData 17 | Peripheral Data |

**Table 5–22: CPU to Mictor connections for Mictor D pins for 405GPASYNC (cont.)**

| Tektronix Mictor D pin number | AMP Mictor D pin number | LA channel | 405GPASYNC signal name | Comments |
|---|---|---|---|---|
| 35 | 08 | D1:7 | PerData 16 | Peripheral Data |
| 36 | 06 | – | – | Not Connected |

## 405GPSDRAM Mictor Connections

Tables 5–23 and 5–24 list the microprocessor signals visible at the mictor connectors.

**Table 5–23: CPU to Mictor connections for Mictor A pins for 405GPSDRAM**

| Tektronix Mictor A pin number | AMP Mictor A pin number | LA channel | 405GPSDRAM signal name | Comments |
|---|---|---|---|---|
| 01 | 01 | – | – | Not Connected |
| 02 | 03 | – | – | Not Connected |
| 03 | 05 | Clock:0 | SysReset~ | SystemReset |
| 04 | 07 | A3:7 | MemData0 | SDRAM Data |
| 05 | 09 | A3:6 | MemData1 | SDRAM Data |
| 06 | 11 | A3:5 | MemData2 | SDRAM Data |
| 07 | 13 | A3:4 | MemData3 | SDRAM Data |
| 08 | 15 | A3:3 | MemData4 | SDRAM Data |
| 09 | 17 | A3:2 | MemData5 | SDRAM Data |
| 10 | 19 | A3:1 | MemData6 | SDRAM Data |
| 11 | 21 | A3:0 | MemData7 | SDRAM Data |
| 12 | 23 | A2:7 | MemData8 | SDRAM Data |
| 13 | 25 | A2:6 | MemData9 | SDRAM Data |
| 14 | 27 | A2:5 | MemData10 | SDRAM Data |
| 15 | 29 | A2:4 | MemData11 | SDRAM Data |
| 16 | 31 | A2:3 | MemData12 | SDRAM Data |
| 17 | 33 | A2:2 | MemData13 | SDRAM Data |
| 18 | 35 | A2:1 | MemData14 | SDRAM Data |
| 19 | 37 | A2:0 | MemData15 | SDRAM Data |
| 20 | 38 | A0:0 | MemData31 | SDRAM Data |
| 21 | A36 | A0:1 | MemData30 | SDRAM Data |

**Table 5–23: CPU to Mictor connections for Mictor A pins for 405GPSDRAM (cont.)**

| Tektronix Mictor A pin number | AMP Mictor A pin number | LA channel | 405GPSDRAM signal name | Comments |
|---|---|---|---|---|
| 22 | 34 | A0:2 | MemData29 | SDRAM Data |
| 23 | 32 | A0:3 | MemData28 | SDRAM Data |
| 24 | 30 | A0:4 | MemData27 | SDRAM Data |
| 25 | 28 | A0:5 | MemData26 | SDRAM Data |
| 26 | 26 | A0:6 | MemData25 | SDRAM Data |
| 27 | 24 | A0:7 | MemData24 | SDRAM Data |
| 28 | 22 | A1:0 | MemData23 | SDRAM Data |
| 29 | 20 | A1:1 | MemData22 | SDRAM Data |
| 30 | 18 | A1:2 | MemData21 | SDRAM Data |
| 31 | 16 | A1:3 | MemData20 | SDRAM Data |
| 32 | 14 | A1:4 | MemData19 | SDRAM Data |
| 33 | 12 | A1:5 | MemData18 | SDRAM Data |
| 34 | 10 | A1:6 | MemData17 | SDRAM Data |
| 35 | 08 | A1:7 | MemData16 | SDRAM Data |
| 36 | 06 | – | – | Not Connected |
| 37 | 04 | – | – | Not Connected |
| 38 | 02 | – | – | Not Connected |

**Table 5–24: CPU to Mictor connections for Mictor C pins for 405GPSDRAM**

| Tektronix Mictor C pin number | AMP Mictor C pin number | Logic analyzer channel | 405GPSDRAM signal name | Comments |
|---|---|---|---|---|
| 01 | 01 | – | – | Not Connected |
| 02 | 03 | – | – | Not Connected |
| 03 | 05 | Clock:3 | MemClkOut | SDRAM Clock |
| 04 | 07 | – | – | Not Connected |
| 05 | 09 | – | – | Not Connected |
| 06 | 11 | – | – | Not Connected |
| 07 | 13 | – | – | Not Connected |
| 08 | 15 | C3:3 | BankSel0~ | Bank Select |

**Table 5–24: CPU to Mictor connections for Mictor C pins for 405GPSDRAM (cont.)**

| Tektronix Mictor C pin number | AMP Mictor C pin number | Logic analyzer channel | 405GPSDRAM signal name | Comments |
|---|---|---|---|---|
| 09 | 17 | C3:2 | BankSel1~ | Bank Select |
| 10 | 19 | C3:1 | BankSel2~ | Bank Select |
| 11 | 21 | C3:0 | BankSel3~ | Bank Select |
| 12 | 23 | C2:7 | DQM0 | Data Mask |
| 13 | 25 | C2:6 | DQM1 | Data Mask |
| 14 | 27 | C2:5 | DQM2 | Data Mask |
| 15 | 29 | C2:4 | DQM3 | Data Mask |
| 16 | 31 | C2:3 | HoldAck | HoldAck |
| 17 | 33 | C2:2 | WE~ | WriteEnable |
| 18 | 35 | C2:1 | CAS~ | ColumnAddress-Strobe |
| 19 | 37 | C2:0 | RAS~ | RowAddressStrobe |
| 20 | 38 | D0:0 | MemAddr0 | SDRAM Address |
| 21 | 36 | D0:1 | MemAddr1 | SDRAM Address |
| 22 | 34 | D0:2 | MemAddr2 | SDRAM Address |
| 23 | 32 | D0:3 | MemAddr3 | SDRAM Address |
| 24 | 30 | D0:4 | MemAddr4 | SDRAM Address |
| 25 | 28 | D0:5 | MemAddr5 | SDRAM Address |
| 26 | 26 | D0:6 | MemAddr6 | SDRAM Address |
| 27 | 24 | D0:7 | MemAddr7 | SDRAM Address |
| 28 | 22 | D1:0 | MemAddr8 | SDRAM Address |
| 29 | 20 | D1:1 | MemAddr9 | SDRAM Address |
| 30 | 18 | D1:2 | MemAddr10 | SDRAM Address |
| 31 | 16 | D1:3 | MemAddr11 | SDRAM Address |
| 32 | 14 | D1:4 | MemAddr12 | SDRAM Address |
| 33 | 12 | D1:5 | MemAddr13 | SDRAM Address |
| 34 | 10 | D1:6 | BA0 | BankAddress |
| 35 | 08 | D1:7 | BA1 | BankAddress |
| 36 | 06 | Clock:2 | ExtAck~ | External Acknowledge |
| 37 | 04 | – | – | Not Connected |
| 38 | 02 | – | – | Not Connected |

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